METHOD, APPARATUS AND COMPUTER PROGRAM PRODUCT FOR EFFICIENT PER THREAD PERFORMANCE INFORMATION

ABSTRACT

A value in a counter on a processor is incremented for occurrences of a monitored event, providing a measured value for the event. The value of the counter register for a first thread is saved responsive to a switch from the first thread to a second thread. The value is saved in an accumulator in system memory. Then, responsive to a switch back to the first thread, the value for the first thread is restored from the accumulator. In this way, a counter may be read, and its value, for the first thread, for example, provides a coherent meaning relative to a previous value for the same thread, despite any intervening thread switches. Since the counter register may be read directly, in the user state, this provides a faster and more consistent means for updating performance counts.